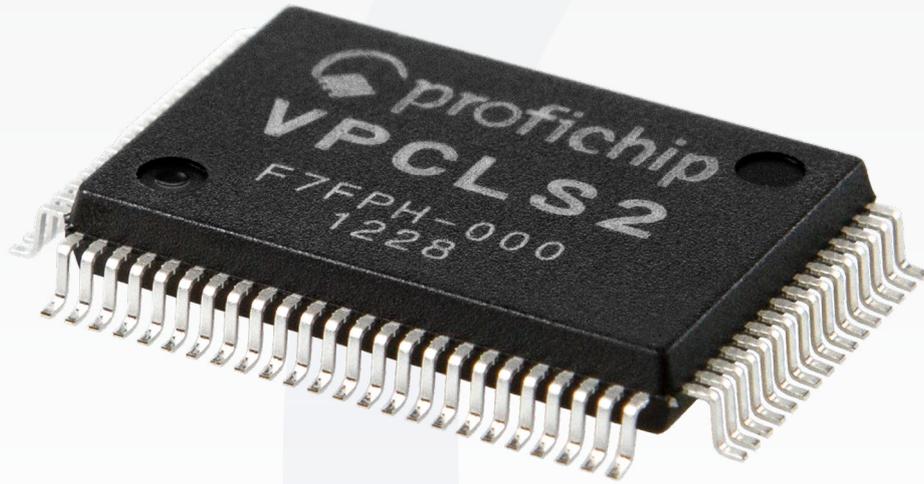# PROFIBUS Lean Slave ASIC

VPCLS2

- Protocol PROFIBUS-DP-V0
- Asynchronous interface according to PROFIBUS-DP
- Maximum data transfer rate 12 Mbit/s
- Automatic recognition of data transfer rate
- 8 bit diagnostic inputs (fixed)
- 32 bits I/O, thereof 16 bits configurable as additional diagnostic inputs
- EEPROM or DIP-Switches are used to set the network address and ID number
- Clock supply 48 MHz
- Supply voltage 5 V
- Pin-compatible with LSPM2 from Siemens
- Package PQFP80 (RoHS compliant)

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Description

The VPCLS2 handles all communication- and diagnosis-tasks of the PROFIBUS-DP-slave-protocol independently. No additional micro-controller or software is needed. All necessary timers and monitoring functions are implemented in hardware. Once the VPCLS2 receives an error-free telegram, it automatically generates the requested response telegram. This ASIC is therfore optimally suited for cost effective single-chip realizations of simple digital PROFIBUS I/O devices.

Operation

The PROFIBUS protocol is handeld by the integrated Microsequencer, a special RISC processor architecture developed by profichip and tailor-made for this type of PROFI-BUS slave applications. The Microsequencer checks all incoming telegrams for correctness and plausibility, monitors the accuracy of the bus timings and automatically generates a response telegram according to the PROFIBUS standard.

Communication features

The Baudrate-Generator provides the internal clocks required for the PROFIBUS transmission rates from 9.6 kbit/s to 12 Mbit/s. The VPCLS2 needs a clock input from an external 48 MHz crystal oscillator. The LSPM2 operation mode with a 24 MHz clock supply and reduced transmission rates is not supported. The I/O interface comprises four 8-bit data ports and one 8-bit diagnostic input port. Each data port may be configured as input or output port. Two data ports can be configured as additional diagnostic input ports. The port direction and its functions are selected by five configuration pins.

Application

The PROFIBUS station address and ID number are stored in an external EEPROM or a serial shift register. The integrated control logic generates the control signals for the serial EEPROM or the external shift register, according to the selected interface type.

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