YASKAWA

ANTAIOS
Feature Set

ANT1000/1001 | Revision 1.02

Liability Exclusion

We have tested the contents of this document regarding agreement with the hardware and software described. Nevertheless, there may be deviations and we do not guarantee complete agreement. The data in the document is tested periodically, however. Required corrections are included in subsequent versions. We gratefully accept suggestions for improvements.

This document is subject to changes without prior notice.

1 Overview

The ANTAIOS is a multi-fieldbus communication chip with dedicated hardware support for (isochronous) real-time Ethernet based protocols.

Based on the approved concept of the SMC1000 chip, which already provides a rich set of communication interfaces, the architecture of the ANTAIOS has been extended by several key features:

- ARM Cortex-A5 Host CPU, 32/32 KB Caches, 288 MHz
- 2 Port Real-Time Ethernet Switch with Integrated PHYs
- 2 Micro-Coded Protocol Processing Unit (PPU) per Ethernet Port
- 1 Additional Protocol Processing Units (PPU)
- PPU Concept: High Performance and Flexibility, Prepared for Other Protocols
- Direct Access from Ethernet Switch (PPU) to SNAP+ Master, Consistency and FIFO Interface and DDR2-SDRAM for Fast and Efficient I/O Data Exchange with Minimum CPU Interaction and System Load
- DDR2 Interface with 200 MHz for Higher Memory Bandwidth
- New NAND–Flash Controller with 16-bit ECC to Support Latest NAND-Flash Technologies
- QuadSPI Controller to Speed-Up Boot Sequence
- Advanced Host Interface for External Processor
- Configurable, FIFO Based Mailbox System for Efficient and Flexible Communication Tasks
- Consistency Interface for Hardware Based Exchange of Consistent I/O Data

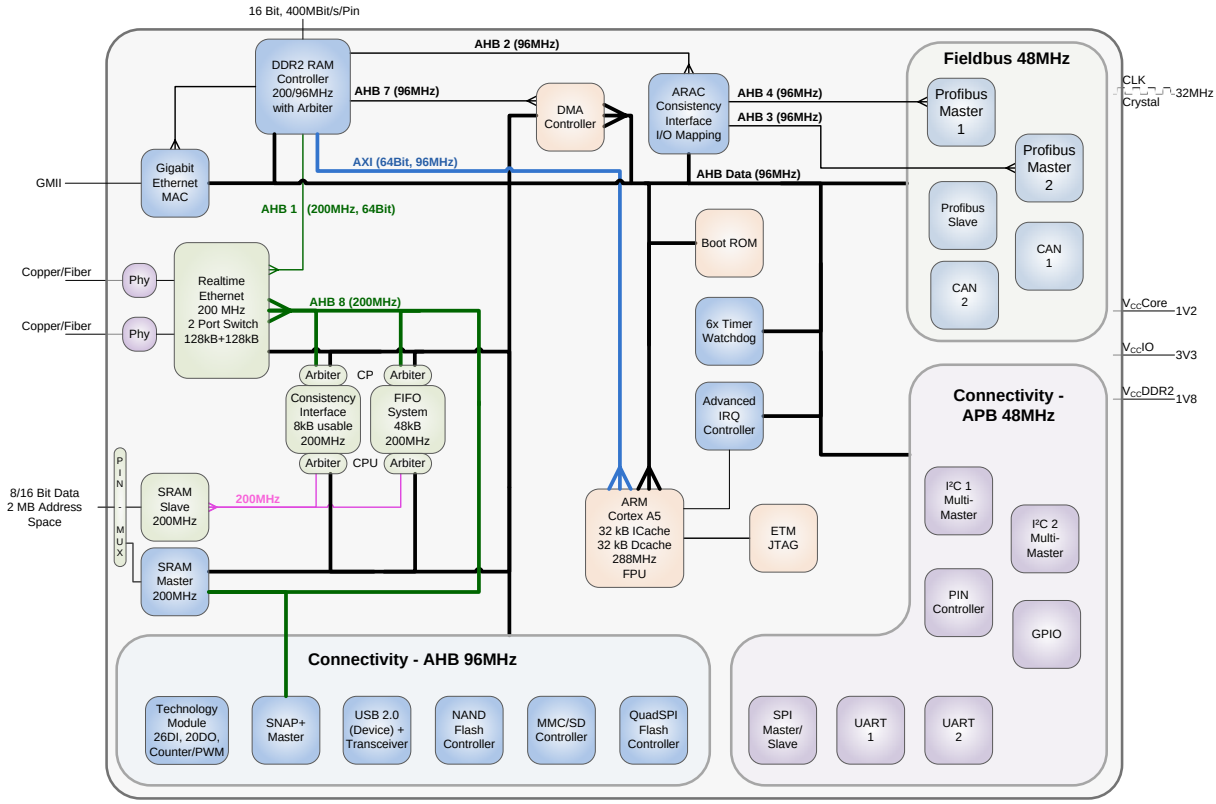
Primary focus of ANTAIOS is the efficient and flexible implementation of high-performance real-time Ethernet communication protocols.

Especially advanced protocols with demanding synchronization mechanisms require dedicated hardware support and shall be addressed with the ANTAIOS chip. These solutions will be based on a combination of micro-coded program execution inside the PPUs for all time critical protocol tasks like synchronization and I/O data exchange, and a high-level protocol stack for non-critical communication tasks (typically provided by a 3rd party cooperation partner).

Pursuing the basic concept of the SMC1000, the ANTAIOS offers several on-chip I/O functions to build block I/Os or small control applications very efficiently. In order to extend the number of I/Os or to realize a modular system concept the integrated SNAP+ Master offers an easy access to profchip’s SliceBus technology.

2 Block Diagram

Figure 2-1 System Overview



3 Key IPs and Features

3.1 ARM Cortex-A5 CPU Core

- 288 MHz Core Speed
- 64-bit AXI
- 32 KByte Instruction Cache
- 32 KByte Data Cache
- JTAG Debug Interface
- ETM (**E**mbedded **T**race **M**acrocell) for Real-Time Tracing
- ITM (**I**nstrumentation **T**race **M**acrocell) for Software Instrumentation
- ETB (**E**mbedded **T**race **B**uffer)
- AHB DAP (**D**ebug **A**ccess **P**ort) for Access of Internal Memory while ARM is Running
- Little Endian Byte Ordering
- 64-bit FPU without NEON

3.2 Advanced Real-Time Ethernet Switch

- 3-Port Switch system to connect two external Ethernet ports with one internal port
- Flexible Architecture Based on a Micro-Coded 5-Core Protocol Processor Unit (PPU) Cluster
- PROFINET® IRT (profichip + Molex)
    - PROFINET IO IRT Specification v2.3
    - Conformance Class C; Real Time Class 3
    - Designed for Cycle Times down to 31.25 µs (High Performance Profile) (Software currently not available for Cycle Times of 31.25 µs)
    - designed for Master and Device
    - Stack: Molex
- MECHATROLINK-III® (Yaskawa)
    - MECHATROLINK-III Master Implementation
    - MECHATROLINK-III Slave Implementation
- EtherCAT® (profichip + Beckhoff)
    - EtherCAT Slave and EtherCAT Master Functionality
    - EtherCAT Technology License Obtained from ETG/Beckhoff
    - EtherCAT Slave Stack by Beckhoff, Support from profichip
- Other planned protocols:
    - EtherNet/IP™ (including CIP Sync™ and DLR)
    - TSN (Time Sensitive Network)
    - Ethernet Powerlink™
    - Modbus® TCP

3.3 Integrated 100Base-TX Ethernet PHYs (2x)

- 2 Integrated 100Base-TX Ethernet PHYs
- 100Base-FX and 10Base-T(e) Support
- Autonegotiation
- Auto MDI/MDIX
- special adaptions made to address profichip's Real-Time requirements

3.4 SNAP+ (SliceBus) Master

(to be used in Combination with SNAP+ ASIC)

- SliceBus Features
  - Single Master System
  - up to 64 Slaves (SNAP+ Modules)
  - Asynchronous, Serial Data Transmission with 48 Mbit/s via Point-to-Point LVDS Physics
- Error Detection Mechanism
  - CRC Code with Hamming Distance 4 for Every Telegram (all 3-bit Errors will be Detected)
  - Watchdog Function inside every SNAP+ Module for SNAP+ Master Observation
  - "Auto Shut Down" in Case of SNAP+ Master Malfunction
  - Retry Statistic for Early Detection of Possible Transmission Issues
- Time-Synchronisation
  - Every SNAP+ Module has its own Clock with 1 µs Resolution
  - All SNAP+ Module Clocks are Synchronized with the SNAP+ Master (Accuracy < 100ns)
  - Option for Clock Synchronization from SNAP+ Master to Fieldbus

- SNAP+ Features (SliceBus Slave ASIC)
  - Technological Functions in SNAP+ ASIC
    - Standard I/O Function: 8 DI/DO or 16 DI or 16 DO with Shift Register
    - Integrated Digital Input Filter Function
    - Asynchronous Event Signalling with µs Time Stamping for Advanced SNAP+ Modules
    - Two Advanced Counters with AB Oversampling, Latch, Reset, Output, Hysteresis, Compare Value, Repetitive/Endless Counting and Additional Time Stamp Information
    - SSI Function with Time Stamp Information (Speed Calculations: Counter Difference/Time)
    - Pulse Width Modulation with 20ns Resolution
    - Frequency Measurement Mode
    - Special Digital I/O Time Stamp Modules (ETS: Edge Time Stamp System) for Input Edge and Output Control with 1 µs Resolution (Independent from Fieldbus Cycle!)
  - SPI Interface in SNAP+ for Analog I/O, Safety I/O or Serial CP with External MCU
    - 2.6 Mbit/s SPI Interface for External Microcontroller
    - Up to 16 Byte IN / 16 Byte OUT Data for External Microcontroller
    - Up to 192 Byte of Parameter Data for External Microcontroller
    - Alarm Function and Watchdog Function

3.5 Gigabit Ethernet MAC

- 10/100/1000 Mbit/s Support
- GMII Support
- DMA Engine for Transmitting and Receiving Packets with Scatter Gather List
- Supports IP, TCP and UDP Checksum Offloads
- IEEE 802.1Q VLAN Tag Insertion for Packet Transmission, VLAN Tag Detection and Removal for Packet Reception

3.6 DDR2 SDRAM Controller (16-bit)

- 800 MByte/s maximum bandwidth
- 200 MHz Clock Rate (400 MHz Data Rate)
- 256 MByte maximum addressable[1)]
- 1 chip select

[1)] For memory configuration see chapter 4.9 in document *ANT1000/1001 Data Sheet*

3.7 Asynchronous External Interface (AEI)

- Configurable 8-bit/16-bit Master and Slave Interface (FIFO / CI)
- Setup, Hold, Access Time and Pause Time Configurable
- 2 Chip Selects with 2 MB Address Range Each and Independent Timings
- 1 Dedicated External IRQ for ARM
- 1 Dedicated External IRQ for SNAP+ Master Synchronization
- Optional WAIT Signal
- Slave Mode with Access Time of 70 ns in Fastest Mode

3.8 FIFO Interface

- FIFO Interface Connected to Real-Time Ethernet Switch, Internal ARM Processor and AEI Slave
- 48 KByte Total Memory, Divided into 256 FIFOs
- 255 IRQ Flags

3.9 Consistency Interface (CI)

- Direct Connection to the Real-Time Switch and the AEI Slave
- 8 KByte Input + 8 KByte Output with Consistency Control
- Byte Reorder Function, e.g.
  - Unaligned Endianness Change with Knowledge of Data Structure
  - Separate PROFINET IOPS/IOCS from I/O Data if required
  - Generate Data Areas with Different Application Update Cycles (e.g. 1 ms and 250 µs for IO Data of One Device)
- 8 Process Image Partitions

3.10 PROFIBUS DP Master (2x)

- 2 Independent PROFIBUS® DP Master
- Compliant with PROFIBUS Standard IEC 61158
- Supports DP-V0, DP-V1, DP-V2 (DxB, IsoM, ClockSync)
- PROFIBUS DP Master Stack Available from profichip/Candeo

3.11 VPC3+ PROFIBUS DP Slave

- PROFIBUS DP Slave with Data Rates up to 12 Mbit/s
- Compliant with PROFIBUS Standard IEC 61158
- 4 KByte Communication RAM
- Supports DP-V0, DP-V1, DP-V2 (DxB, IsoM, ClockSync)
- Hardware-PLL for DP-V2 IsoM
- Hardware Synchronization Signal to SNAP+ Master

3.12 CAN Interface (2x)

- FullCAN Controller for Data Rates up to 1 Mbit/s
- Complies with CAN Standard ISO 11898
- Up to 15 Messages Simultaneously (Each with Maximum Data Length)
- Different Message Buffers Can Be Combined as FIFO
- Listen Only Mode (Monitoring of the CAN-Bus, No Acknowledge, No Error Flags)
- Support of Clock Synchronization Between ANTAIOS Based Stations

3.13 NAND-Flash Controller

- 8-bit NAND-Flash Controller
- DMA Capable in Conjunction with Main DMA Controller
- ECC: 16-bit Correctable for 512 Byte

3.14 QuadSPI Interface

- Max. 96 MHz per 4-line (max. 384 Mbit/s)
- DMA Mode
- Programmable Serial Bit Clock Polarity, Phase and Frequency
- SPI Serial Mode, Dual Mode and Quad Mode
- Additional Optional 4th Address Byte (Extend Address Space up to 4096 M)
- 2 Chip Select Lines

3.15 SD/MMC Card Controller

- Supports the MMC Bus Protocol, Version 4.3
- Compliant with the SD Memory Card Protocol Version 3.0
- Write Protect Pin
- Card Detect Pin
- Integrated DMA Controller
- Built-in Generation and Check for 7-bit and 16-bit CRC Data
- 1 KByte FIFO Buffer
- 4-bit Mode
- High Speed 25 MByte/s possible

3.16 USB 2.0 Device Controller

- USB 2.0 High Speed Device Controller (480 Mbit/s)
- 8 Endpoints
- Integrated USB PHY

3.17 Advanced IRQ Controller

- 8 Priority Levels
- Round-Robin Option for IRQs with the Same Priority
- Throttling Option for Every IRQ Channel
- All IRQs Can Be Masked
- 32-bit ISR Vector for Each IRQ
- Configurable Input Filters for External IRQs
- IRQ/FIQ Selectable for Each IRQ Channel

3.18 Main DMA Controller

- Scatter/Gather Capable with Chained Transfer (Linked List)
- 8 DMA channels
- Support for Fixed Source Address (Read from Auto-Increment-Register) to Memory
- Support for Reading from 8-bit Device and Copy to 32-bit Device

3.19 AHB/APB Bridge (2x)

- DMA channels

3.20 SPI Interface

- Master Mode with up to 80 Mbit/s
- Slave Mode with up to 24 Mbit/s
- DMA Mode in Conjunction with APB-Bridge
- Programmable Frame/Sync. Polarity
- Programmable Serial Bit Clock Polarity, Phase and Frequency
- Programmable Serial Bit Data Sequence (MSB or LSB First)
- 2 Chip Select Lines

3.21 UART (2x)

- Standard Features (Compatible to 16C550):
  - 5/6/7/8 Data Bits
  - 1/1.5/2 Stop Bits
  - None/Odd/Even/Stick Parity
  - Register/FIFO Mode
  - Line Break Generation & Detection
  - Programmable Baud Rate Generator
  - Fully Prioritized Interrupt System Controls
  - Status Reporting Capabilities
  - Modem Control Functions
  - Loopback Mode
- Enhanced Features:
  - High Speed Mode for Higher Baud Rates up to 12 Mbit/s
  - Module Controlled Activation/Deactivation for RTS
  - 32-Byte FIFO with 16C650 DMA Behaviour
  - DMA Mode in Conjunction with APB-Bridge
  - Enable/Disable Receiver
  - IRQ Generation by Extended Timeout Control/Detection
  - IRQ Generation by Two Configurable ETX Characters
  - IRQ Generation by Receive Byte Counter
  - IRQ Generation by Transmitter with Selectable “THR Empty” or “TSR Empty”

3.22 I²C Interface

- Master or Slave for the I²C bus
- Data is Transmitted to and Received from the I²C Bus via a Buffered Interface
- Supports the Standard and Fast Modes
- Supports the 7-bit, 10-bit, and General-Call Addressing Modes
- Glitch Suppression by Debounce Circuit
- Programmable Slave Address
- Supports the Master-Transmit, Master-Receive, Slave-Transmit, and Slave-Receive Modes
- Supports the Multi-Master Mode
- General-Call Address Detection in the Slave Mode
- Supports system manager Bus 2.0 in Master and Slave Modes
- Supports All System Manager Bus 2.0 Protocol Commands Except Quick Command and Host Notify Protocol

3.23 Timer and Watchdog Module

- Timer
  - Six Independent 32-bit Timer with pre-scaler (10 ns – 80 ns Selectable)
  - Interrupt can be issued upon overflow and time-up
  - Each timer has two compare registers
  - Supports increment and decrement modes
  - Six interrupt sources, one for each counter/timer
  - Supports single-shot and free running mode
  - Automatically reloaded when reaching zero
- Watchdog
  - 32-bit Down Counter with Prescaler
  - Access Protection
  - Mode 1: System Reset or IRQ at Watchdog Event
  - Mode 2: Watchdog IRQ at First Watchdog Event, System Reset at Next Watchdog Event (Can Be Used for Debugging)
  - Option to Pass Information through the System Reset: Two Registers with POWER-ON-RESET Only (not Affected by Watchdog-Reset)

3.24 Boot Code

- Boot Option Selectable by GPIOs
- Boot from QuadSPI NOR-Flash
- Boot from NAND-Flash
- Boot from UART 1
- Boot from Parallel NOR-Flash

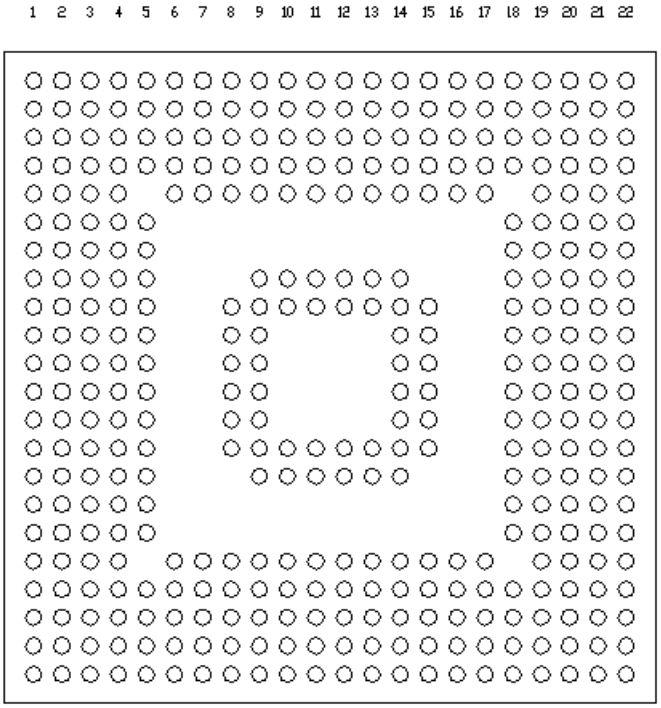
3.25 Technology Function Module (TechIO)

- Max. 26 Bits Input and 20 Bits Output (Shared with Other Interfaces)
- Configurable Digital Input Low Pass Filter
- Up to 4 Counter Channels with Quadruple Evaluation for Incremental Encoders
- Up to 4 PWM Channel (**P**ulse **W**idth **M**odulation)
- Up to 2 SSI Encoder Interfaces

3.26 Package 1

- TFBGA-380
- 15 x 15 mm² with ball pitch 0.65 mm
- profichip order code: ANT1000

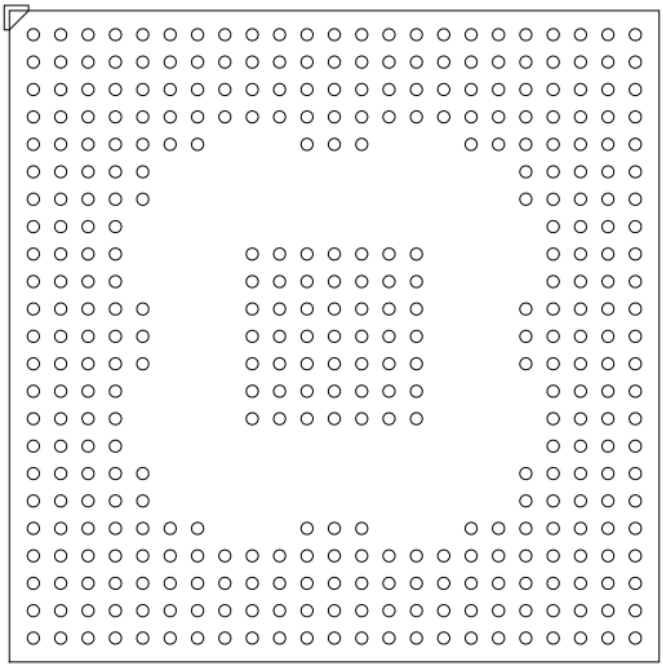
Figure 3-1 TFBGA-380 Bottom View



3.27 Package 2

- TFBGA-385
- 19 x 19 mm² with ball pitch 0.8 mm
- profichip order code: ANT1001

Figure 3-2 TFBGA-385 Bottom View



4 Revision History

Table 4-1 Revision history

Version	Date	Remarks
V0.10	07.12.2012	First release
V0.11	09.12.2012	Overview added
V0.12	06.02.2014	Complete review and update
V0.13	25.09.2014	Added 64kByte Caches and new size of FIFO and CI
V0.14	29.09.2014	Update to Overview Image
V0.15	30.09.2014	added Package Drawing, corrected TechIOs
V0.16	09.10.2014	Corrected Number of UARTs to 2, added comments to CI, FIFO and USB
V0.17	01.04.2015	FA616 replaced by ARM Cortex-A5
V0.18	24.9.2015	Added debug options to CA5, Changed frequencies of SPI, Added second Package Option
V0.19	25.01.2016	Changed small Package
V0.20	15.06.2016	Updated package 2
V0.21	16.06.2016	Minor corrections, block diagram updated, order information added
V0.22	10.11.2016	New document design
V0.23	22.02.2017	content updated
V1.00	27.02.2017	Release 2017.02.27
V1.01	19.05.2017	Changed document title
V1.02	01.10.2019	New document design

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